

A product specification entitled "IMAGINE: The Image Engine --

419 Documentation & User's Manual" (version 2.80), provides additional details of embodiments of the data processing circuit 1 and is incorporated herein by reference and is appended as an annex to this specification.

IN THE CLAIMS:

Please cancel claims 1-3, 5-17 and 21-25 without prejudice.

Please add the following new claims:

1 26. (New) A processor comprising:
2 a plurality of functional units;
3 a bus structure including a plurality of buses, including a bus for each of the
4 functional units; and
5 a plurality of bus registers, each coupled to an output of only a corresponding
6 one of the plurality of functional units and to only a corresponding one of the plurality
7 of buses.

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1 27. (New) A processor as recited in claim 26, wherein the plurality of functional units
2 comprises:
3 a multiplier unit; and
4 an arithmetic logic unit (ALU);
5 such that a first bus register of the plurality of bus registers is coupled to an
6 output of the multiplier and to a first bus of the plurality of buses, and a second bus
7 register of the plurality of bus registers is coupled to an output of the ALU and to a
8 second bus of the plurality of buses.

1 28. (New) A processor as recited in claim 27, wherein the multiplier unit and the ALU
2 are each adjustable to operate upon data words of any of a plurality of different lengths,
3 the plurality of different lengths being integer multiples of each other.

1 29. (New) A processor as recited in claim 28, wherein the data words are integer data
2 words.

1 30. (New) A processor as recited in claim 29, wherein the plurality of different lengths
2 are multiples of eight bits.

1 31. (New) A processor as recited in claim 28, wherein the ALU has at least three
2 operand inputs.

1 32. (New) A processor as recited in claim 31, further comprising a control register
2 containing a plurality of bits which define a three port parametrised logic function to be
3 performed on the at least three operand inputs, the ALU receiving a plurality of bits
4 from the control register to execute the three port parametrised logic function.

1 33. (New) A processor as recited in claim 27, wherein the plurality of functional units
2 further comprises a shift register, such that a third bus register of the plurality of bus
3 registers is coupled to an output of the shift register and to a third bus of the plurality of
4 buses.

1 34. (New) A processor as recited in claim 33, wherein the plurality of functional units
2 further comprises a register bank including a plurality of registers on which operations
3 are to be performed, such that a fourth bus register is coupled to a first one of the
4 plurality of registers and to a fourth bus of the plurality of buses, and a fifth bus register
5 is coupled to a second one of the plurality of registers and to a fifth bus of the plurality
6 of buses.

1 35. (New) A processor comprising:
2 a multiplier unit adjustable to multiply integer data words of any of a plurality of
3 different lengths, the plurality of different lengths being integer multiples of each other;
4 an arithmetic logic unit (ALU) adjustable to perform arithmetic operations on
5 integer data words of any of the plurality of different lengths;
6 a shift register;
7 a bus structure including a plurality of buses, including a bus for each of the
8 multiplier unit, the ALU, and the shift register; and
9 a plurality of bus registers, each coupled to an output of a separate
10 corresponding one of the multiplier unit, the ALU, and the shift register and to a
11 separate corresponding one of the plurality of buses.

10
11 36. (New) A processor as recited in claim 35, wherein the plurality of different lengths
1 are multiples of eight bits.

1 37. (New) A processor as recited in claim 35, wherein the ALU has at least three
2 operand inputs.

1 38. (New) A processor as recited in claim 37, further comprising a control register
2 containing a plurality of bits which define a three port parametrised logic function to be
3 performed on the at least three operand inputs, the ALU receiving a plurality of bits
4 from the control register to execute the three port parametrised logic function.

1 39. (New) A processor as recited in claim 35, wherein the plurality of functional units
2 further comprises a register bank including a plurality of registers on which operations
3 are to be performed by the multiplier, the ALU or the shifter, and wherein the plurality
4 of bus registers includes a first bus register coupled to a first one of the plurality of
5 registers in the register bank and to a first one of the plurality of buses, and a second
6 bus register coupled to a second one of the plurality of registers in the register bank and
7 to a second one of the plurality of buses.

1 40. (New) A circuit for processing integer data for graphic image processing
2 applications, comprising:

3 a multiplier unit having a pipeline to multiply integer data words of 8 bits or
4 multiples thereof, the pipeline being adjustable to the length of the integer data words
5 to be multiplied;

6 an arithmetic logic unit (ALU) to perform arithmetic operations on integer data
7 words of 8 bits or multiples thereof, the word length of the ALU being adjustable in
8 accordance with the multiple of 8 bits constituting the integer data words;

9 a register unit including at least two registers to store integer data words on
10 which a multiplication or arithmetic operation is to be performed; and

11 a bus structure including a plurality of buses, including a bus for each of the
12 multiplier, the ALU, and each of the at least two registers; and

13 a plurality of bus registers, each coupled to an output of a separate
14 corresponding one of the multiplier, the ALU, and each of the at least two registers, and
15 each coupled to a separate corresponding one of the plurality of buses.

1 41. (New) A circuit as recited in claim 40, further comprising a shift register, wherein
2 the plurality of bus registers includes an bus register coupled to an output of the shift
3 register and to a corresponding one of the plurality of buses.

1 42. (New) A circuit as recited in claim 41, wherein the ALU has at least three operand
2 inputs.

1 43. (New) A circuit as recited in claim 42, further comprising a control register
2 containing a plurality of bits which define a three port parametrised logic function to be
3 performed on the at least three operand inputs, the ALU receiving a plurality of bits
4 from the control register to execute the three port parametrised logic function.
